Novel LTCC/BGA Modules for Highly Integrated Millimeter-Wave Transceivers

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***Abstract*—Advanced packaging concepts for highly integrated encapsulated millimeter-wave modules are demonstrated. Millimeter-wave monolithic integrated circuits (MMICs) are flip-chip mounted on top of a low-temperature co-fired ceramic (LTCC) package. This type of "smart package" can integrate various passive functions as well as compact interconnections between MMIC and vertical feedthroughs. The bottom side of this package is connected via a standard ball grid array (BGA) to a low-cost laminate printed circuit board serving as a motherboard for multiple LTCC modules. Fabricated passive LTCC test structures fully validate the approach for millimeter-wave applications. LTCC-/BGA-based packages feature good performance up to approximately 30 GHz. Alternatively to BGA technology, anisotropic conductive pastes are applied as well. They have proven to be suitable at least up to 40 GHz.**

***Index Terms*—Ceramics, millimeter-wave integrated circuits, multichip modules, packaging.**

I. Introduction

IN ORDER TO make millimeter-wave electronics for commercial applications such as microwave radio or automotive radar a successful high-volume product, low-cost manufacturing and high integration are essential. Low-temperature co-fired ceramic (LTCC) technology, today widely used for frontend modules for price-sensitive applications like mobile phones [1], [2], is very well suited to meet these requirements. It offers a great potential for passive integration, even up to millimeter-wave frequencies, where, so far, almost exclusively thin-film alumina substrates have been used. Recent work on LTCC modules has demonstrated solutions for 5-GHz wireless local-area network (LAN) [3]–[5] and Ku-band V-SAT [6] applications. These first-generation transceiver modules leave further potential for much higher integration. With continuously improving LTCC production technologies [7], it becomes feasible to realize fully integrated millimeter-wave modules of compact size as small as a fingernail. Advanced packaging techniques, already used in mass production of chip-size surface acoustic wave (SAW) filters [8], [9], can be applied to these LTCC modules, such that a compact encapsulation with excellent hermetic sealing is obtained at very low cost. Furthermore, millimeter-wave transceivers can be split into functional blocks being realized as a surface-mountable device (SMD)-type package for a single 26.5-GHz millimeter-wave monolithic integrated circuit (MMIC) has already been presented in [10]. Due to the chosen single-layer laminate, passive drop-on components inside the package walls were still needed. The LTCC module approach presented in [11] offers much higher passive integration and more compact packaging opportunities for future miniaturized millimeter-wave transceiver modules. The approach discussed in [11] is further pursued here. In addition, vertical feedthroughs and buried transitions are investigated both analytically and experimentally. The range of LTCC test packages and modules is extended.

Manuscript received April 16, 2003.

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Digital Object Identifier 10.1109/TMTT.2003.819210

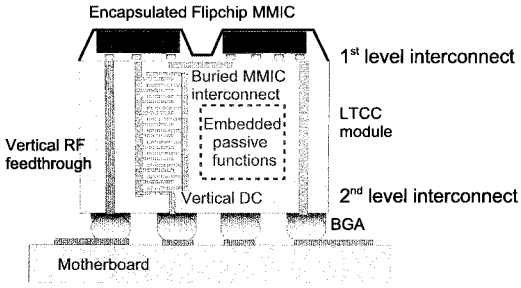


Fig. 1. LTCC module.

II. Module Architecture

Fig. 1 illustrates the proposed module concept. The top and bottom LTCC layers host the first- and second-level interconnects, respectively. All necessary transitions between the MMIC or feedthroughs from the top to bottom layer are vertically integrated inside the LTCC.

Hence, interference with the proposed hermetic encapsulation having a metal shielding in close proximity to the LTCC top surface is avoided. The inner space of the LTCC is allocated for passive functions like filters, couplers, or RF-blocking capacitors. The bottom side of this package is connected to a low-cost laminate printed circuit board (PCB) serving as motherboard for multiple LTCC modules. The interconnects (second level) consist of solder balls with standard ball grid array (BGA) pitch dimensions of 500 or 800 μm. They exhibit good performance from dc up to millimeter waves, as was shown in [12] and [13]. In conjunction with LTCC, this paves the way for high-volume production technology, as will be shown in this paper. The more sophisticated micro-BGAs (μBGAs), suggested in [3] for stacked LTCC modules, are thus not required in the present context.

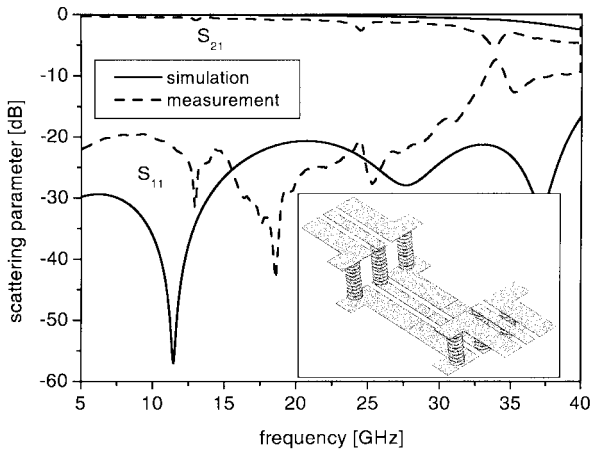


Fig. 2. Vertical three-wire feedthrough.

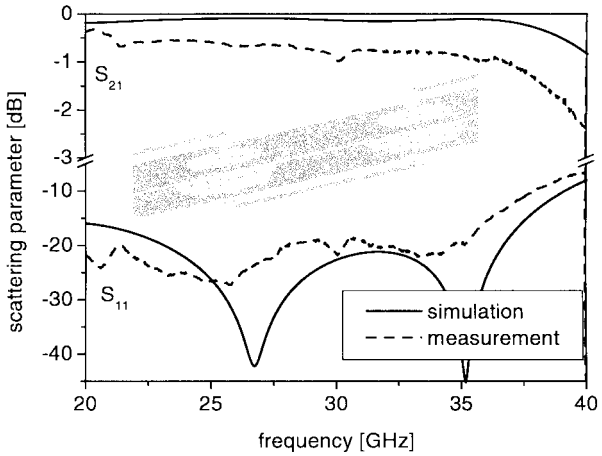


Fig. 3. Quasi-coaxial vertical feedthrough.

The following LTCC layer topology is considered for the designs described below. The substrate consists of 12 dielectric layers having a dielectric constant $\varepsilon_r = 7.8$ (K8). The two outer layers are 38-μm thick, the remaining ten inner ones are 55 μm. 10-μm-thick conductors are printed in between the layers with minimum linewidth and spacing of 100 μm. Vertical transitions are realized using vias of 100-μm diameter being interlinked on adjacent layers with catchpads of 200-μm diameter.

III. Three-Dimensional (3-D) Integrated Passive Functions

Key components of such an LTCC module are vertical feedthroughs and buried transitions. The former connect the top surface of the LTCC carrying the active devices with the bottom side. There, input and output pads for RF, as well as dc and control signals are located. RF feedthroughs especially represent a design challenge because they must establish a proper millimeter-wave connection. Indeed, they lead the RF signal through all the dielectric layers of the LTCC module. The buried transitions interconnect the MMIC mounted on top of the LTCC module. Here, impairment of their electrical performance by shielded encapsulants on the surface must be avoided. Compact low-loss solutions for these feedthroughs and buried transitions are discussed below.

A. Vertical Feedthroughs

The simplest possible feedthrough between a coplanar waveguide (CPW) on the top and bottom LTCC layer can be realized by a vertical three-wire structure. Fig. 2 shows a corresponding back-to-back configuration with CPW feed lines on the top layer. The simulated and measured performance are shown for a via pitch of 500 μm. This value was found to be optimum from a full-wave analysis. The overall area of a single vertical feedthrough designed for the substrate described above is 1.2×0.2 mm^2. The simulation of such a back-to-back configuration on a module of $4 \times 4 \times 0.626$ mm^3 shows low input reflection ($S_{11} \leq -20$ dB) and high transmission ($S_{21} > -1$ dB) up to millimeter waves. Measurements were performed on such a module not yet separated from a complete test panel consisting of several test structures. These results confirm the functionality of such a feedthrough up to approximately 30 GHz. A large discrepancy between measurement and simulation is observed above 33 GHz. Resonances occur hinting at unwanted modes propagating in the test panel.

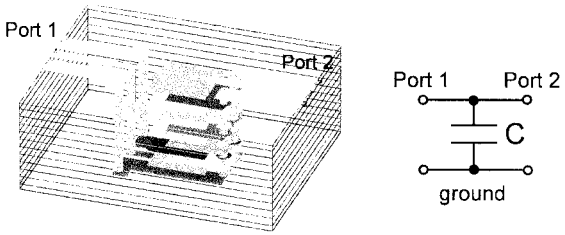


Fig. 4. RF-blocking capacitor test structure and its simplified equivalent circuit.

Performance enhancement can be achieved by additional shielding of the vertical feedthrough. Fig. 3 depicts the setup and performance of a quasi-coaxial vertical feedthrough. Again, the setup is arranged in a back-to-back configuration. It is fed by a 235-μm-wide microstrip with its ground plane on the fourth metallization layer from the surface. The resulting thickness of 203 μm leads to a 50-Ω line. The feedthrough consists of a center via led through holes in the ground planes. It is encircled by eight shielding vias between the ground planes. In a full-wave analysis, the optimum radius was determined to 500 μm. There is a very good agreement between measurement and simulation. The measured input reflection S_{11} remains below -20 dB (-10 dB) up to 35 GHz (40 GHz). The transmission S_{21} is better than -0.5 dB (-1 dB) up to 37 GHz (40 GHz) per transition.

The performance of these compact vertical feedthroughs is further validated experimentally in Section IV-A.

B. Embedded RF-Block Capacitors

In order to achieve an integrated dc supply with a shunt RF-blocking capacitor, an interdigital arrangement of parallel plates, as sketched in Fig. 1, is evaluated. Such LTCC-integrated capacitors can replace chip capacitors, which usually are extra components that have to be placed on top of the substrate. Fig. 4 shows the structure connected via a vertical three-wire structure and feed lines allowing two-port on-wafer

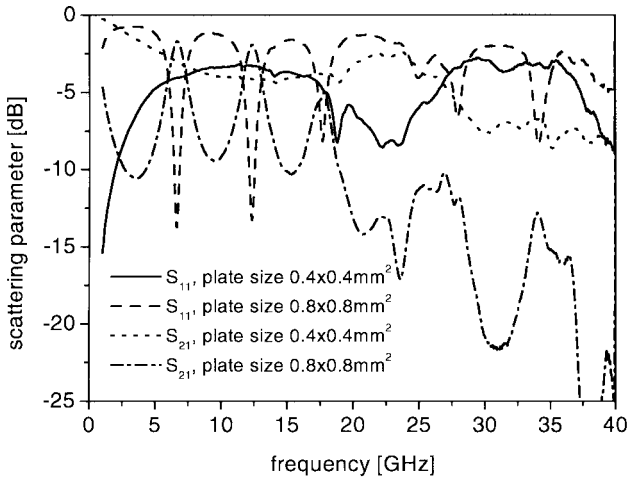


Fig. 5. Measured scattering parameters of RF-blocking capacitors with different plate sizes.

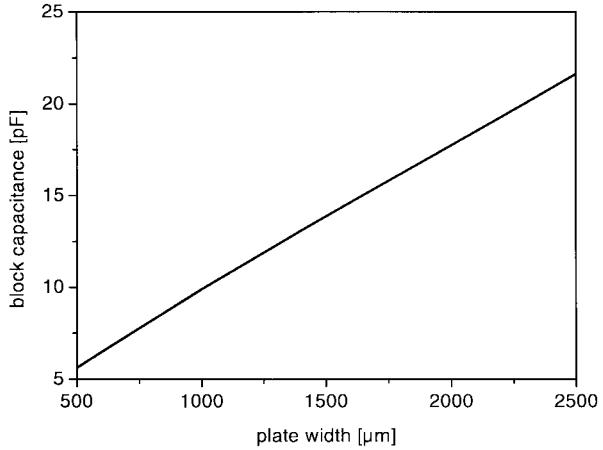


Fig. 6. Extracted blocking capacitance values.

characterization on the same layer. Its simplified equivalent circuit is also shown for a better understanding.

Fig. 5 shows the measured scattering parameters for RF blocks with different plate sizes. As expected, increasing the plate area shifts the blocking performance to lower frequencies. For the larger plate sizes, the input reflection S_{11} is approximately -1 dB at 2 GHz, while the transmission drops below -10 dB. At higher frequencies, parasitic resonances occur.

Here, the maximum achievable capacitance is limited to a few picofarads by the number of layers and the low dielectric constant (K8) of the used LTCC substrate. Higher capacitance values can be achieved by further increasing the plate size. The extracted low-frequency blocking capacitances for different plate sizes are shown in Fig. 6. The plate length is set to 0.8 mm, while the width is varied. These values still offer an acceptable overall size of the RF-blocking capacitor when compared to standard MMIC dimensions. When thinner layers and higher dielectric constant materials (K20, K80) for these RF-blocking capacitors are used, much larger capacitance values can be achieved.

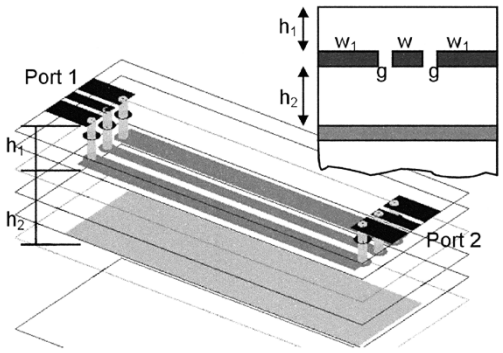


Fig. 7. Buried MMIC interconnection.

TABLE I
DIFFERENT BURIED LINE CONFIGURATIONS

$50\,\Omega$ type	A	B	C	D
w [μm]	150	150	150	150
w_1 [μm]	300	300	300	300
g [μm]	120	150	170	120
h_1 [μm]	93	93	38	203
h_2 [μm]	165	110	110	165

C. Buried MMIC Interconnections

Buried transitions between MMICs are not necessarily top-to-bottom interconnections. In order to leave as many layers as possible available for further passive integration of other structures such a buried chip-to-chip interconnect (BCCT) should ideally occupy only little space in the vertical and lateral directions. Triplates and striplines were found to be rather unqualified because of their overall size. Following standard design rules for a 50-Ω triplate and stripline with a reasonable conductor linewidth of 100 μm, the distance between the shielding grounds is 500 and 800 μm, respectively. Therefore, only buried coplanar lines are considered for interconnections, as they are very compact. Their fields are concentrated at the slots. Good isolation between the interconnection and other adjacent passive integrated components is automatically given, thus, the occupied space is minimized. The buried CPW with an additional ground plane, depicted in Fig. 7, is vertically interconnected by vias to two 50-Ω CPW feed lines on top.

Four different configurations labeled A–D to realize buried 50-Ω lines are investigated. The parameters defining the structure (see Fig. 7) are summarized in Table I. For these transitions, the overall depth still offers reasonable space for passive integration underneath the shielding ground plane.

In order to check for length resonances due to mismatch at the vias, the buried line length is varied from 0.7 to 4 mm. Fig. 8 shows the simulated scattering parameters for all line types.

The buried line length is 0.7 mm in the depicted case. The input reflection S_{11} remains below -10 dB for all investigated line types, while the transmission S_{21} is better than -1 dB at frequencies up to 40 GHz. These findings also hold for the simulations with all the other line lengths not shown here. Test structures for evaluation of the designed BCCT are fabricated using the EPCOS LTCC process. Corresponding reference lines and

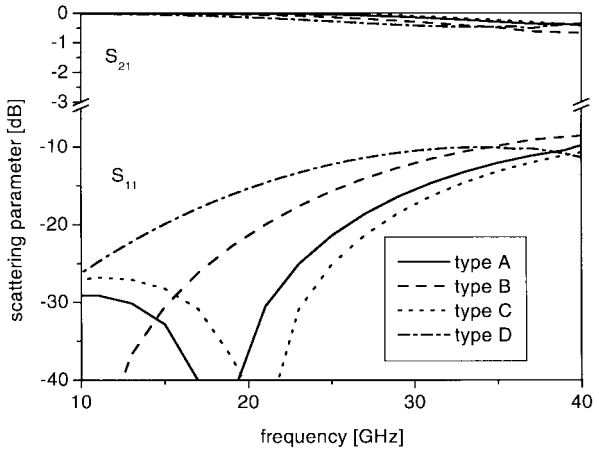


Fig. 8. Simulated scattering parameters for different buried line types.

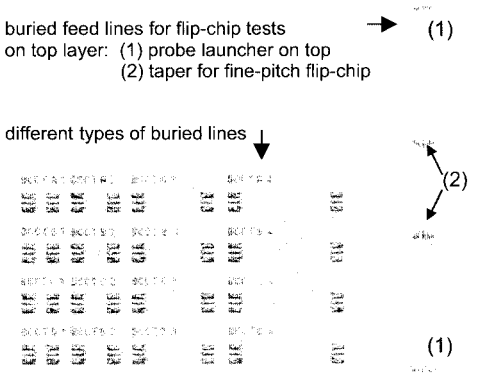


Fig. 9. Two subregions of a fabricated LTCC panel.

thru-reflect-line (TRL) calibration standards are added to the LTCC panel as well. Fig. 9 illustrates two subregions of the realized panel. The left-hand-side one shows BCCT test structures. The top layer is fully visible, while the buried lines only partly shine through. The other structure in the right-hand side of Fig. 9 is suitable for flip-chip tests described later in this section.

Fig. 10 shows the results for all line types A–D with the same buried line length of 0.7 mm. The measured scattering parameters compare quite well with the simulated results (Fig. 8). The input reflection S_{11} remains below -10 dB, while the transmission S_{21} is on the order of -1 dB up to 40 GHz. The functionality of these transitions is also validated for the other line lengths. The results are not depicted here.

In order to meet the above-mentioned requirements, good transmission and low-input reflection are not sufficient. In addition, the influence of a metal shielding near the surface needs to be low. The scattering parameters are thus measured with a copper plate positioned above the buried lines (line length 4 mm) for all types A–D. In the following, results for two cases are discussed in more detail. Line types C and D are compared, corresponding to minimum and maximum buried depth, respectively. The variation of the scattering parameter S_{21} when added a cover plate is depicted in Fig. 11.

In Fig. 11(a) ($|\Delta|S_{21}||$), the absolute value of the deviation of the magnitude (in decibels) is plotted versus frequency, while Fig. 11(b) depicts $|\Delta\phi_{21}|$, the absolute value of the phase difference. Obviously, the cover plate influences the impedance and electrical length of the buried line, the effect being more pronounced the closer the buried CPW is to the surface. However, even for the smallest buried depth realizable in the chosen layer configuration (type C, $h_1 = 38\ \mu$m), the deviation is still tolerable, especially when taking into account that line lengths are much shorter than 4 mm in typical applications. As expected,

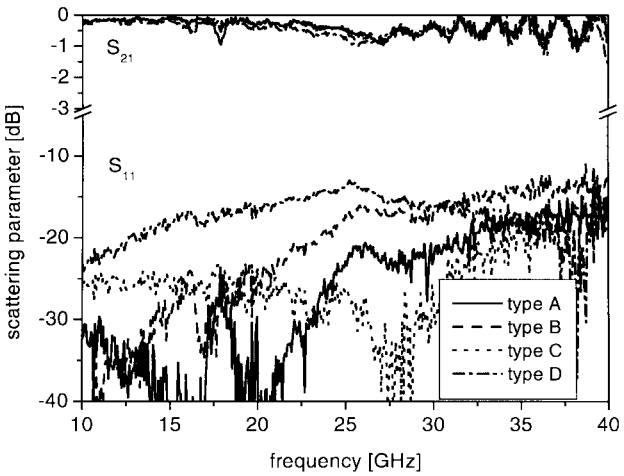
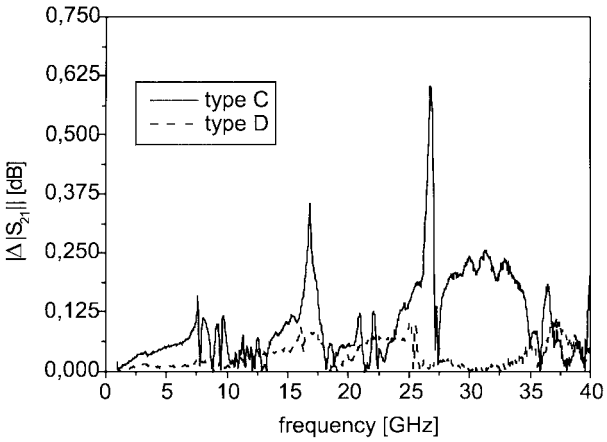
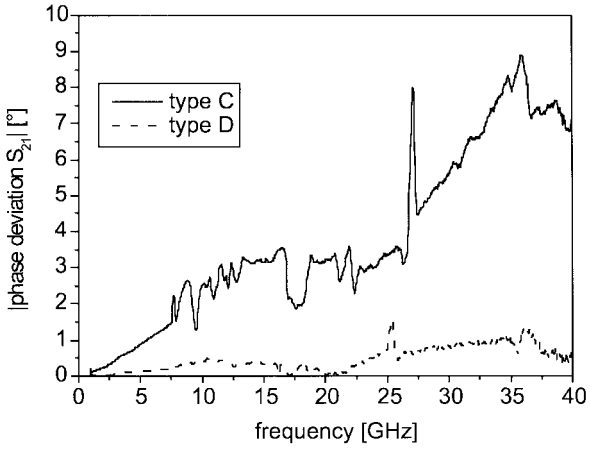


Fig. 10. Measured scattering parameters for different buried line types.

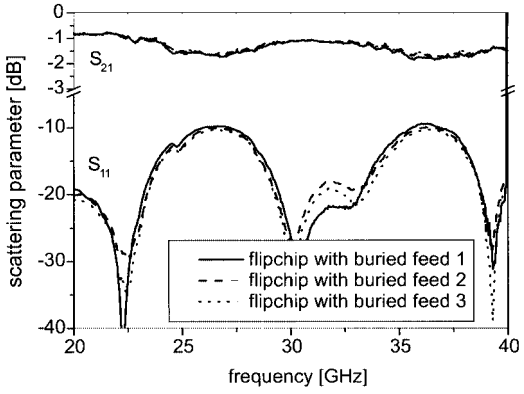


(a)

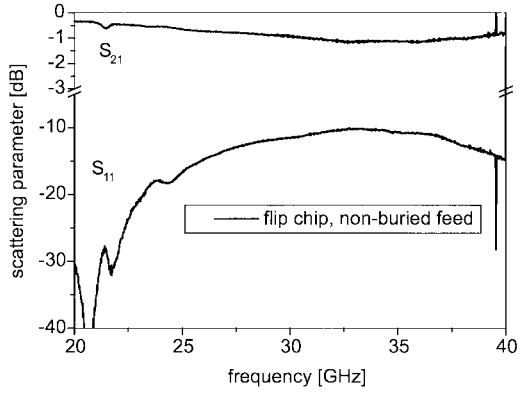


(b)

Fig. 11. Measured influence of a metal cover plate on S_{21} of the buried lines. (a) Magnitude and (b) phase difference.

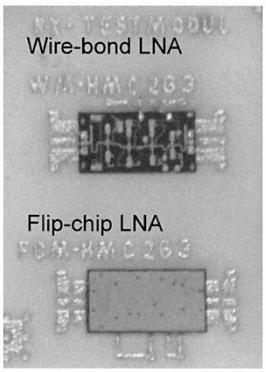


(a)

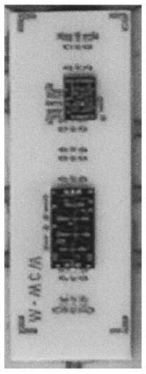


(b)

Fig. 12. Measured performance of flip-chip test devices with: (a) a buried feed line and (b) a feed line on top.



(a)



(b)

Fig. 13. (a) Realized LNA modules. (b) Full receiver module.

the deviations for the other lines (types A and B) remain between the two extremes depicted in Fig. 11. The corresponding scattering parameters are, therefore, not shown. Furthermore, it was found that the influence on the input reflection S_{11} is negligible for all types.

Next, the flip-chip test structures are characterized. They consist of two buried lines, which can be interconnected via a flip-chip test device. To this end, the CPW lines on the top layer are tapered to standard fine pitch dimensions (pad-to-pad distance of 150 μm). 50-Ω CPW lines fabricated on a 127-μm ceramic substrate serve as flip-chip test devices in the experiments. These test chips are stud-bumped and thermo-compression bonded to the LTCC so as to bridge the gap between the two buried lines. Three identical configurations are assembled to check for reproducibility. For comparison reasons, flip-chip arrangements without buried feed lines are also assembled. Scattering-parameter measurements are performed by means of vector network analysis (VNA) utilizing a Cascade Microtech probe station with CPW probes. Fig. 12(a) shows the measured results for the three flip-chip configurations with a buried feed. Fig. 12(b) demonstrates the performance of the same kind of test chip when it is connected with 500-μm-long feed lines placed on top.

Although the flip-chip arrangement is not optimized for low-input reflection, the comparison of these results shows that applying the buried chip-to-chip transitions does not degrade the overall performance. In both cases, the input reflection S_{11} remains below -10 dB. The slightly increased transmission loss in Fig. 12(a) can be related to the additional length of a buried line of 4 mm on each side of the flip-chipped CPW line. These results also show that fine-pitch flip-chip assemblies are feasible with this standard LTCC process.

IV. Realized Test Modules and Packages

In order to experimentally evaluate the performance of these packaging and interconnection concepts, several test packages are fabricated using EPCOS' commercial LTCC process. An LNA, as well as a receiver module and several other test packages with various integrated passive functions and interconnects, are assembled and tested. The LTCC packages are mounted on the laminate via standard BGA technology. Alternatively, also anisotropic conductive pastes (ACPs) are investigated to build the second-level interconnect.

A. LTCC Amplifier Module

Hittite's HMC263 MMIC LNA is used as the active chip device. LTCC modules are designed for both flip-chip and wire-bond assembly of the MMIC on top of the LTCC substrate. Fig. 13(a) shows the realized modules. In each layout, the center region below the MMIC is occupied by two RF blocking capacitors (Section III-B). Furthermore, CPW lines on the top layer in the outer left- and right-hand-side parts of the modules are visible. They are connected to the bottom layer by vertical three-wire structures (Section III-A). This type of feedthrough is preferred for its higher flexibility with regard to wire-bond or flip-chip assembly.

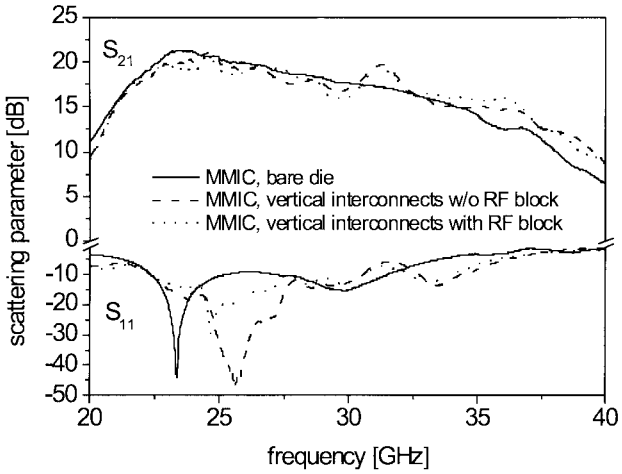


Fig. 14. Measured performance of an LNA in different configurations.

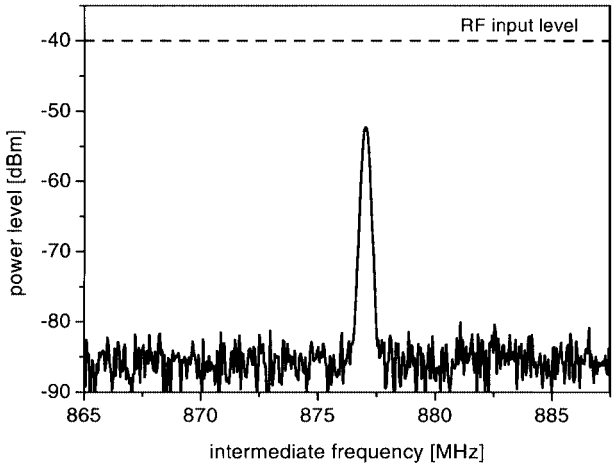


Fig. 15. Measured performance of mixer connected via buried MMIC interconnections.

Each module offers several pads for probing purposes on the top and bottom layers. For comparison, the same MMIC was measured in a bare die configuration and via vertical interconnects. By simply removing or adding wire bonds on the top layer, these different circuit configurations can easily be realized. Fig. 14 shows the measured performance of the 26.5-GHz LNA mounted in wire-bond technology for the following circuit configurations. First, the bare MMIC mounted on top of the module is measured. This MMIC is then wire bonded to vertical interconnects for RF signal transmission and dc supply without a shunt RF block capacitor. Finally, the dc supply bonds are rerouted to vertical dc supplies with an integrated shunt capacitor. Connecting the MMIC via the various vertical interconnects does not degrade the chip performance. For all circuit configurations, the measured performance meets the chip specification (i.e., between 24–27 GHz: min. (typ.) gain 20 (25) dB; min. (typ.) input return loss 4 (7) dB). In comparison to the bare MMIC, the transmission S_{21} is only slightly attenuated (worst case: 2 dB) in the operating band. This total insertion loss is given by the two vertical three-wire feedthroughs plus the wire bonds.

B. LTCC Receiver Module

Fig. 13(b) shows the LNA MMIC in combination with Hittite's HMC264 mixer MMIC. Both are mounted on a single LTCC substrate building a fully integrated multichip receiver module. The LTCC contains vertical RF and dc feedthroughs, as well as buried MMIC interconnections, as introduced in Section III-C. Again, additional pads are provided for probing purposes. These were used to test the mixer MMIC in combination with the buried MMIC interconnections. Fig. 15 shows the measured IF signal of the mixer MMIC. All RF signals (RF input at 26.5 GHz and subharmonically pumped local oscillator (LO) input at approximately 12.75 GHz) are led to the MMIC via the buried MMIC interconnections. The measured conversion loss (CL) is approximately 12 dB. Compared to the chip specifications $(\mathrm{CL} = 10\ \mathrm{dB})$, this means an additional loss of 2 dB that is attributed to the losses introduced by the buried feed lines.

These examples clearly demonstrate the full functionality of the built LTCC modules. Next, the interface to the motherboard PCB will be investigated.

C. LTCC BGA Package

Test packages for verification of the second-level interconnects based on standard BGAs are realized. LTCC packages consisting of a CPW line on top vertically fed by a three-wire feedthrough at each end are fabricated using two different designs. In the first design, the via pitch of the three-wire structure is set to 500 μm. For this value, the transmission characteristic of the vertical interconnect was found to be optimum (refer to Section III-A). This value also correlates with the desired minimum pitch for a standard BGA suitable for mass production. In the second design, the optimum via pitch of 500 μm is tapered to a BGA pitch of 800 μm within the lower LTCC layers. This is another standard value in mass production. To this end, the distance between the two outer vias and the center via is increased in the last three layers. Interconnection of the stacked vias is provided by adequate cover pads on the metallization layers in between. These LTCC packages are mounted on a low-cost laminate suitable for millimeter-wave applications. Here, Rogers' Ro4003 is chosen. The substrate with a dielectric constant $\varepsilon_r = 3.38$ is 200-μm thick. Both sides have 35-μm-thick copper cladding. In order to keep the overall size of transmission lines on Ro4003 small, microstrip lines $(\text{width} = 465\ \mu\text{m})$ are preferred rather than CPW. Suitable transitions from the microstrip line to CPW are then required for the second-level interconnects and for CPW probe launchers. Different CPW-to-microstrip transitions on Ro4003 are designed. The ground connection is achieved by quarter-wave (radial) stubs, by 200-μm filled vias, or by a combination of both. The quarter-wave stubs are designed for 26.5 GHz, leading to a stub length of approximately 1800 μm. Fig. 16(a) depicts such landing structures on Ro4003 before the LTCC package is mounted. A resist mask is printed on the Ro4003 in order to limit the solder flow. It consists of circles with an outer and inner radius of 400 and 150 μm,

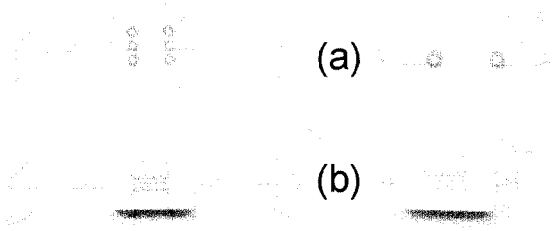


Fig. 16. LTCC test packages mounted on an Ro4003 substrate using standard BGA technology.

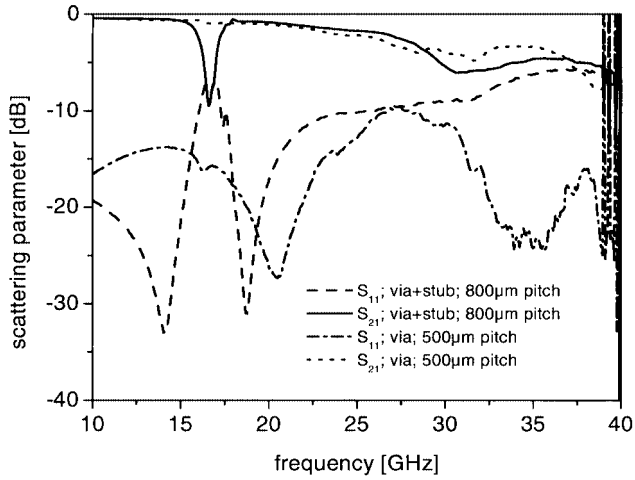


Fig. 17. Measured scattering parameters of 500- and 800-μm-pitch BGA packages.

respectively. Due to the local character of the solder resist mask, its influence on the RF performance should be low, as predicted by simulations.

Solder is applied to the vertical three-wire structure at the bottom side of the LTCC leading to a ball with approximately 300-μm diameter attached to each vertical interconnect after heating. These LTCC packages are placed on the Ro4003 substrate such that each ball is surrounded by a solder resist circle. This arrangement is finally assembled in a reflow process. Different LTCC test packages are mounted on various landing structures with a BGA pitch of 500 and 800 μm, respectively. The 500-μm BGA pitch packages are shown in Fig. 16(b). Measurement results for both BGA pitches are depicted in Fig. 17.

In all cases, a TRL calibration is performed to eliminate the influence of the probe launchers. Due to the chosen calibration standards, this can successfully be performed up to 38 GHz. The resonance at 17 GHz is due to the simultaneous use of quarter-wave stubs and vias for the CPW-to-microstrip transitions. For the 500-μm BGA pitch with two different CPW-to-microstrip transitions, the input reflection S_{11} remains below -10 dB. The overall transmission S_{21} is better than -2 dB $(-3$ dB$)$ up to 27 GHz $(30$ GHz$)$. This leads to a low transmission loss of approximately 1 dB per BGA transition. The measurements of the 800-μm BGA pitch setups also show good results up to 30 GHz. This experimental study illustrates the feasibility of this packaging approach, which exclusively relies on standard BGA and LTCC technologies.

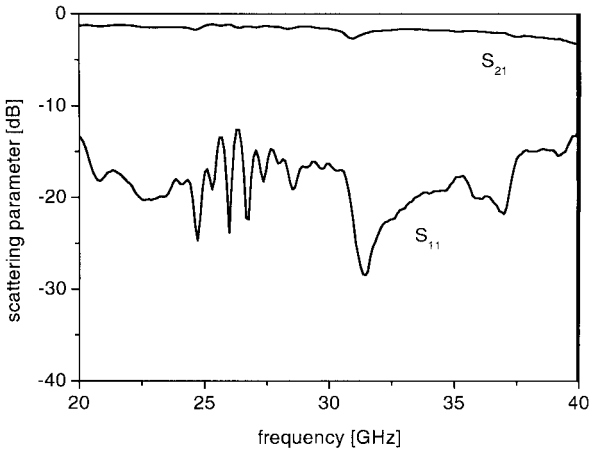


Fig. 18. Measured scattering parameters of the ACP package.

D. LTCC ACP Package

For applications beyond 30 GHz, solder balls with smaller nonstandard dimensions or different materials are required. The tradeoff between short interconnection length for good RF performance and sufficient height to account for thermal coefficient of expansion (TCE) mismatch at the PCB interface has to be carefully considered though.

Here, conductive adhesives serving as second-level interconnects are discussed. They are applied between the LTCC module and PCB instead of the solder balls. ACPs particularly seem to offer a promising alternative to BGA technology when it comes to higher frequencies. They consist of gold polymer-filled epoxy. The conductive particles in the epoxy are coated with a thin dielectric layer. When pressure is applied to the ACP, the gold particles get in contact where they are squeezed. At the exposed areas, their thin coating is destroyed. This direct contact provides electrical conductivity in the vertical direction (direction of pressure), while in the lateral direction, isolation is still guaranteed by the remaining coating. The achievable pitch for this application depends on the diameter of the coated gold balls in the epoxy. Here, Loctite's 3440 single-component heat-cure gold polymer-filled epoxy is applied to mount the LTCC packages described in Section IV-C on the Ro4003 substrate. The required pitch of 500 μm for these packages can be easily achieved with this ACP (the gold ball diameters are less than 30 μm). Thus, the minimum achievable pitch of these second-level interconnects is basically determined by the LTCC design rules. Hence, with these alternative technologies, higher integration densities at the module–PCB interface can be achieved at low cost. ACP is dispensed in a single step to the landing structures on the Ro4003 substrate. Isolation of adjacent pads is fully provided by the anisotropic characteristic of the adhesive. After mounting the LTCC package on the laminate, the arrangement is cured for 60 s at 180 °C and 13.8 bar pressure. Fig. 18 depicts scattering-parameter measurements performed on such an ACP test package. The input reflection S_{11} remains well below -10 dB up to 40 GHz, while the overall transmission loss does not exceed 2 dB up to 37 GHz. This means very low insertion loss of less than 1 dB per transition up to 40 GHz. In summary, the functionality of the LTCC module approach pursued here

can be extended well beyond 30 GHz by applying alternative low-cost technologies for the second-level interconnect.

V. Conclusion

LTCC-based millimeter-wave package solutions with embedded passive functions have been presented. Various vertical top-to-bottom feedthroughs and buried MMIC transitions have been realized. The chosen packaging approach enables advanced encapsulations technologies up to millimeter waves. These LTCC modules can be mounted on a low-cost laminate PCB using a standard BGA interface, which demonstrates good performance up to 30 GHz. Beyond 30 GHz, anisotropic conductive adhesives offer an alternative also adaptable to mass production. The functionality of the proposed packaging concepts is fully validated by scattering-parameter measurements performed up to 40 GHz on passive and MMIC-mounted LTCC test modules and packages. All modules presented here are fabricated in EPCOS' 8-in high-volume LTCC process.

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